WHAT IS CLAIMED IS:

1. A clock and data recovery (CDR) device capable of recovering a clock from data transmitted at a variable data rate, the CDR device comprising:

a reference clock generating section arranged to generate a reference clock corresponding to the variable data rate in accordance with a control signal;

a clock and data recovery section arranged to receive the transmitted data, recover a clock and data from the received data and output the recovered clock and data; and

a control section arranged to generate the control signal according to the variable data rate and send the control signal to the reference clock generating section.

2. The CDR device according to claim 1, wherein said reference clock generating section comprises:

a basic clock generator arranged to generate a basic clock as an internal clock;

a first divider arranged to divide the basic clock generated by the basic clock generator by a first value P set by the control section;

a frequency detector arranged to compare the divided basic clock with an output signal of a multiplier and output an error there between;

a loop filter arranged to filter an error signal output from the frequency detector and compensate for a feedback loop;

a first voltage-controlled oscillator arranged to extract a phase-synchronized clock under the control of the loop filter; and

a multiplier arranged to multiply the synchronized clock output from the first voltage-controlled oscillator by a second value Q set by the control section to output the reference clock.

3. The CDR device according to claim 1, wherein said clock and data recovery section comprises:

a NRZ (No Return to Zero)-PRZ(Pseudo Return to Zero) converter arranged to convert an NRZ signal having no clock component into a PRZ signal including a clock component and outputting the PRZ signal;

a phase/frequency detector arranged to compare the reference clock output from the reference clock generating section with a clock component of the signal outputted from the NRZ-PRZ converter to detect a phase error there between, compare a clock of a signal outputted from a second divider, which has been produced by dividing an output clock of a second voltage-controlled oscillator by a third value M set by the control section, with the clock component of the signal outputted from the NRZ-PRZ converter to detect a frequency error there between, and output the frequency error;

a filter arranged to filter the frequency error and compensate for a feedback loop;

a second voltage-controlled oscillator arranged to output a phase-synchronized clock according to the control of the filter;

a second divider arranged to divide the synchronized clock outputted from the second voltage-controlled oscillator by a third value M which is set by the control section and output the divided clock; and

an output section arranged to receive NRZ data and the synchronized clock output from the second voltage-controlled oscillator and output a combined a clock and data signal.

4. The CDR device according to claim 2, wherein said clock and data recovery section comprises:

a NRZ (No Return to Zero)-PRZ(Pseudo Return to Zero) converter arranged to convert an NRZ signal having no clock component into a PRZ signal including a clock component and outputting the PRZ signal;

a phase/frequency detector arranged to compare the reference clock output from the reference clock generating section with a clock component of the signal outputted from the NRZ-PRZ converter to detect a phase error there between, compare a clock of a signal outputted from a second divider, which has been produced by dividing an output clock of a second voltage-controlled oscillator by a third value M set by the control section, with the clock component of the signal outputted from the NRZ-PRZ converter to detect a frequency error there between, and output the frequency error;

a filter arranged to filter the frequency error and compensate for a feedback loop;

a second voltage-controlled oscillator arranged to output a phase-synchronized clock according to the control of the filter;

a second divider arranged to divide the synchronized clock outputted from the second voltage-controlled oscillator by a third value M which is set by the control section and output the divided clock; and

an output section arranged to receive NRZ data and the synchronized clock output from the second voltage-controlled oscillator and output a combined a clock and data signal.

5. The CDR device according to claim 2, wherein the reference clock is calculated by the equation:

f_{ref} = (basic clock) x (Q/P) (wherein P and Q are parameters set by the control section).

6. The CDR device according to claim 3, wherein said filter is a PID (Proportional Integral Differential) filter.

7. The CDR device according to claim 3, wherein said output section is a D-flip-flop.

8. The CDR device according to claim 4, wherein said filter is a PID (Proportional Integral Differential) filter.

9. The CDR device according to claim 4, wherein said output section is a D-flip-flop.

10. A method for recovering a clock from data transmitted at a variable data rate, the method comprising the steps of:

generating a control signal based upon the data rate signal of a received data signal;

generating a reference clock in accordance with the control signal;

recovering a clock and data from the received data signal; and

outputting the recovered clock and data.

11. The method according to claim 10, wherein said generating step includes:

generating a basic clock as an internal clock;

dividing the basic clock by a first value P which is part of the control signal;

comparing the divided basic clock with an output signal of a multiplier and outputting an error there between;

filtering the error signal and compensating for a feedback loop;

extracting a phase-synchronized clock under the control of the loop filter; and

multiplying the synchronized clock, using the multiplier, by a second value Q which is part of the control signal.

12. The method according to claim 10, wherein said recovering step includes:

converting an NRZ signal having no clock component into a PRZ signal including a clock component and outputting the PRZ signal;

comparing the reference clock with the clock component to detect a phase error

there between, comparing a clock of a signal outputted from a divider, which has been produced by dividing an output clock of a voltage-controlled oscillator by a third value M set which is part of the control signal, with the clock component to detect a frequency error there between, and outputting the frequency error;

filtering the frequency error and compensating for a feedback loop;

outputting a phase-synchronized clock, by the voltage-controlled oscillator, according to the control of the filter;

dividing, by the divider, the synchronized clock outputted from the voltage-controlled oscillator by a third value M which is part of the control signal and outputting the divided clock;

receiving NRZ data and the synchronized clock outputted from the voltage-controlled oscillator; and

outputting the NRZ data and the synchronized clock as a combined clock and data signal.